

Claims

What is claimed is:

1. A method of making a semiconductor device, comprising:
 - forming a drain region;
 - forming an epitaxial region having a first conductivity type over the drain region;
 - forming a source region over a first portion of the epitaxial region;
 - forming a gate region over a second portion of the epitaxial region;
 - forming a first region disposed within the epitaxial region and under the gate region, wherein the first region has a first doping concentration of a second conductivity type opposite the first conductivity type;
 - and
 - forming a second region disposed under the first region, wherein the second region has a second doping concentration of the second conductivity type which is less than the first doping concentration.
2. The method of claim 1, further including:
 - forming a trench into the epitaxial region; and
 - disposing the gate region within the trench.
3. The method of claim 1, wherein the first conductivity type is N-type semiconductor material.
4. The method of claim 1, wherein the first region is made with P+ semiconductor material.

5. The method of claim 1, wherein the second region is made with P- semiconductor material.

6. A semiconductor device having a gate region, comprising:

an epitaxial region having a first conductivity type;

a first region disposed within the epitaxial region and under the gate region, wherein the first region has a first doping concentration of a second conductivity type opposite the first conductivity type; and

a second region disposed under the first region, wherein the second region has a second doping concentration of the second conductivity type which is less than the first doping concentration.

7. The semiconductor device of claim 6, further including a trench formed in the epitaxial region for disposing the gate region within the trench.

8. The semiconductor device of claim 6, further including:

a drain region disposed below the epitaxial region; and

a source region disposed over a first portion of the epitaxial region.

9. The semiconductor device of claim 6, wherein the first conductivity type is N-type semiconductor material.

10. The semiconductor device of claim 6, wherein the first region is made with P+ semiconductor material and the second region is made with P- semiconductor material.

11. The semiconductor device of claim 6, wherein the semiconductor device is a junction field effect transistor.

12. A semiconductor device having a gate region, comprising:

an epitaxial region having a first conductivity type;

a first region disposed within the epitaxial region and under the gate region, wherein the first region has a first doping concentration of a second conductivity type opposite the first conductivity type; and

a second region disposed adjacent to a first portion of the first region, wherein the second region has a doping concentration of the second conductivity type which is less than the first doping concentration.

13. The semiconductor device of claim 12, further including a third region disposed adjacent to a second portion of the first region, wherein the third region has a doping concentration of the second conductivity type which is less than the first doping concentration.

14. The semiconductor device of claim 12, further including a trench formed in the epitaxial region for disposing the gate region within the trench.

15. The semiconductor device of claim 12, further including:

a drain region disposed below the epitaxial region; and

including a source region disposed over a first

portion of the epitaxial region.

16. The semiconductor device of claim 12, wherein the first conductivity type is N-type semiconductor material.

17. The semiconductor device of claim 12, wherein the first region is made with P+ semiconductor material and the second region is made with P- semiconductor material.

19. The semiconductor device of claim 12, wherein the semiconductor device is a junction field effect transistor.

20. A semiconductor device, comprising:

- a first gate region;

- an epitaxial region having a first conductivity type; and

- a first region disposed within the epitaxial region, under the first gate region and extending at least half way through the epitaxial region, wherein the first region has a second conductivity type opposite the first conductivity type.

21. The semiconductor device of claim 20, further including:

- a second gate region; and

- a second region disposed within the epitaxial region, under the second gate region and extending at least half way through the epitaxial region, wherein the second region has the second conductivity type.

22. The semiconductor device of claim 21, further including a third region disposed between the first and

second regions and having the first conductivity type.

23. The semiconductor device of claim 20, further including a trench formed in the epitaxial region for disposing the first gate region within the trench.

24. The semiconductor device of claim 20, further including:

 a drain region disposed below the epitaxial region;
and

 a source region disposed over a first portion of the epitaxial region.

25. The semiconductor device of claim 20, wherein the first conductivity type is N-type semiconductor material.

26. The semiconductor device of claim 20, wherein the first region is made with P+ semiconductor material.

27. The semiconductor device of claim 20, wherein the semiconductor device is a junction field effect transistor.

28. A transistor having a gate region, drain region, and source region, comprising:

 an epitaxial region having a first conductivity type; and

 a semiconductor material disposed within the epitaxial region, under the gate region and extending into the epitaxial region of sufficient depth to reduce drain to source resistance of the transistor, wherein the semiconductor material has a conductivity type which is opposite the first conductivity type.

29. The transistor of claim 28, wherein the semiconductor material includes:

a first region disposed within the epitaxial region, under a first portion of the gate region and extending at least half way through the epitaxial region; and

a second region disposed within the epitaxial region, under a second portion of the gate region and extending at least half way through the epitaxial region.

30. The transistor of claim 29, further including a third region disposed between the first and second region and having the first conductivity type.

31. The transistor of claim 28, wherein the semiconductor material includes:

a first region disposed within the epitaxial region and under the gate region, wherein the first region has a first doping concentration of a second conductivity type opposite the first conductivity type; and

a second region disposed under the first region, wherein the second region has a doping concentration of the second conductivity type which is less than the first doping concentration.

32. The semiconductor device of claim 28, wherein the semiconductor device is a junction field effect transistor.